Name: Gabriele Provana
Job title: Head of Infrastructure Operations & Delivery
Title of the Talk: Green, Blue and Business
Abstract: (TBD)
Short Bio: Senior manager in the Information & Communication Technology and digital services sector with more than twenty years of experience in energy, industrial, commercial and international contexts.
Born in Crema in 1968, he graduated in Electronic Engineering at the Politecnico di Milano, specializing in mobile robotics and artificial intelligence.
Since 2015 he has been heading the ICT infrastructures of the Eni group. He is a worldwide manager of IT, TLC, digital services for people and Eni's Green Data Center.
In 20 years of experience as manager of application and infrastructural development and management, he has led business units of information systems in the chemical, refining, power generation, environmental management, trading and supply sectors, through major programs for the transformation of information systems in the Eni group.

Names: Enrico Bazzi and Alessandro Maggio
Job titles: Chief Operating Officer and Chief Marketing & Digital Officer, Jakala
Title of the Talk: Metaverse for Brands
Abstract: Hype or Reality? What strategy ought to be used? What capabilities do we need? These are the reoccurring questions that CMOs ask themselves on the daily, given that they find themselves in a dynamic and culturally ever-changing context, powered by a never-ending technological evolution. The aim of this course, in fact, is to touch on the following points:

1. What is the metaverse
2. What are the main trends
3. What are successful examples of use cases
4. What are the possible strategic approaches
5. What capabilities are required

Short bios: Enrico Bazzi is currently Chief Operating Officer of JAKALA Group, where he started his professional path as CEO of the former Marketing Solutions Division. After a long experience in international groups as a Sales Manager, he developed strong expertise in marketing innovation, loyalty programs, customer engagement, and business strategy. He is committed to supporting the strong JAKALA international growth path, with a focus on enhancing the brand positioning among customers and prospects in Eastern Europe.
With over 25 years of experience in managerial roles within the digital, media and marketing functions, Alessandro Maggio worked in multinational and multicultural brands and consulting companies, across different industries, developing the ability to think at high strategic level and, in the same time, to lead the execution at granular level, with pragmatism, positive sense of urgency and togetherness.

Name: Stanislav Bohm
Job title: Senior Researcher, IT4Innovations
Title: How to use HPC and not go crazy
Abstract: Running jobs on HPC systems can be challenging, especially with heterogeneous systems and complex workflows.
This talk will provide an overview of these difficulties and what can go wrong. It will demonstrate the use of HyperQueue as a solution to these problems. HyperQueue is a lightweight system that can be easily deployed on an HPC system and that simplifies task submissions and resource management.

HyperQueue will also be demonstrated in a hands-on exercise and this talk serves as a basic introduction. The speaker is one of the main authors of HyperQueue.
Short Bio: Stanislav Böhm is currently a senior researcher at the National Supercomputing Centre IT4Innovations. He is an active developer interested in distributed systems, machine learning and verification.

Name: Ryan Kastner
Job Title: Professor, UC San Diego
Title of the talk: Higher-Level Synthesis
Abstract: (TBD)
Bio: (TBD)

Name: Jeronimo Castrillon
Job title: Professor, TU Dresden
Title of the talk: Compiling for heterogeneous platforms
Abstract: After a quick review of the fundamentals of compilers, this lecture introduces auto-parallelising approaches, such as polyhedral compilation, as an attempt to automatically generate efficient code for parallel execution. We discuss how these methods, alone, fall short to cope with the increasing heterogeneity of computing systems to motivate the recent rise of higher-level programming abstractions and compiler frameworks such as MLIR. The lecture provides various examples of programming flows for heterogeneous systems, with an in-depth dive into abstractions for tensor expressions as vehicle to optimize for modern reconfigurable hardware, for emerging memory technologies and for emerging in-memory computing.
Short bio: Jeronimo Castrillon is a professor in the Department of Computer Science at the TU Dresden, where he is also affiliated with the Center for Advancing Electronics Dresden (CfAED). He is the head of the Chair for Compiler Construction, with research focus on methodologies, languages, tools and algorithms for programming complex computing systems. He received the Electronics Engineering degree from the Pontificia Bolivariana University in Colombia in 2004, his masters degree from the ALaRI Institute in Switzerland in 2006 and his Ph.D. degree (Dr.-Ing.) with honors from the RWTH Aachen University in Germany in 2013. In 2014, Prof. Castrillon co-founded Silexica GmbH/Inc, a company that provides programming tools for embedded heterogenous architectures, now with Xilinx/AMD.

Name: Fabrizio Ferrandi
Job title: Associate professor, Politecnico di Milano
Title of the talk: Bambu: high-level synthesis for complex heterogeneous applications
Abstract: Applications operating on very large datasets present unique behaviors, such as fine-grained, unpredictable memory accesses and highly unbalanced task-level parallelism, that make existing high-performance general-purpose processors or accelerators (e.g., GPUs) suboptimal. Various custom accelerator designs for this application area, including solutions based on reconfigurable devices (Field Programmable Gate Arrays), try to address these issues. These new approaches often employ High-Level Synthesis (HLS) to accelerate the development of the accelerators. This lecture presents Bambu, an open-source framework for research in high-level synthesis. It leverages existing software compilers (GCC and CLANG/LLVM) to generate FPGA-based accelerators directly from C/C++/MLIR/LLVM specifications. The Bambu high-level synthesis approach will be discussed and put into perspective by presenting critical technologies for an efficient accelerator synthesis, starting from how MLIR could be used as a higher-level specification going through the low-level accelerator integration problem.

Short bio: Fabrizio Ferrandi (Member, IEEE) received the Laurea (cum laude) degree in electronic engineering and the Ph.D. degree in information and automation engineering (computer engineering) from the Politecnico di Milano, Milan, Italy, in 1992 and 1997. He has been an assistant professor with the Politecnico di Milano, until 2002. Currently, he is an associate professor with the Dipartimento di Elettronica, Informazione e Bioingegneria of the Politecnico di Milano. His research interests include synthesis, verification simulation, and testing of digital circuits and systems. He is a member of the IEEE Computer Society since 1995, the Test Technology Technical Committee, and the European Design and Automation Association.

Name: Dieter Kranzlmueller
Job title: Professor / Director
Title of the talk:
The Future of Supercomputing is Acceleration
Abstract: Supercomputers are an essential tool of science and research today. Many of the most challenging research questions can only be tackled with powerful high performance computers. Unfortunately, the demand for power always exceeds the available capabilities, even though we are now entering the exascale era. Indeed, todays supercomputers face two major challenges: power consumption and the predicted end of Moore's law. This calls for new solutions with respect to energy efficiency as well as the use of accelerators in modern supercomputer architectures. This talk will provide use cases of HPC, a quick overview of European developments, and introduction to energy efficient supercomputing, and last but not least the utilization of quantum accelerators for future integrated supercomputers.
Short bio: Dieter Kranzlmueller is a full professor of Computer Science at the Ludwig-Maximilians-Universitaet (LMU) Munich and chairman of the board of directors of the Leibniz Supercomputing Center (LRZ) of the Bavarian Academy of Sciences and Humanities. He serves on a number of boards, including the national Gauss Center for Supercomputing (GCS) and the Center for Digital Technology & Management (CDTM).

Name: Luca Caviglione
Job title: Senior Research Scientist, Italian National Research Council
Title of the Talk: Shut Up `n Hide Yer Data
Abstract: the increasing complexity of hardware and software platforms jointly with the unbounded growth of data volumes lead to an attack surface difficult to control. A recent trend is the use of information hiding and steganographic techniques to create advanced threats able to covertly exfiltrate data, obfuscate their presence, retrieve malicious payloads, or bypass security execution enclaves. However, the ability of cloaking arbitrary information by leveraging the load of data characterizing modern applications can be also exploited to protect computing platforms and trace the diffusion of scientific results. As a consequence, the security of advanced, heterogenous and data-intensive applications needs a partial rethink. In this perspective, this talk will focus on the dual nature of information hiding and steganography. First, it will present hazards to be considered when developing mission-critical and sensitive applications. Then, it will discuss techniques that can be used to face the new-wave of hazards targeting scientific experiments and "as-a-Service" frameworks.
Short Bio: Luca Caviglione s a Senior Research Scientist at the Institute for Applied Mathematics and Information Technologies of the National Research Council of Italy. He holds a Ph.D. in Electronic and Computer Engineering from the University of Genoa, Italy. His research interests include optimization of large-scale computing frameworks, traffic analysis, wireless and heterogeneous communication architectures, and network security. He is the author or co-author of more than 150 academic publications, and several patents

in the field of p2p and energy-aware computing. He has been involved in Research Projects and Network of Excellences funded by the ESA, the EU and the MIUR. He is also a contract professor in the field of networking/security and a board member for the PhD program in Security, Risk and Vulnerability of the University of Genoa (Cybersecurity and Reliable AI). He is the head of the IMATI Research Unit of the National Inter-University Consortium for Telecommunications, part of the Steering Committee of the Criminal Use of Information Hiding initiative, and a work group leader of the Italian IPv6 Task Force

Name: Lana Josipović
Job title: Assistant professor, ETH Zurich
Title of the talk: From C/C++ code to high-performance dataflow circuits
Abstract: High-level synthesis (HLS) tools generate digital hardware designs from high-level programming languages (e.g., C/C++) and promise to liberate designers from low-level hardware description details. Yet, HLS tools are still acceptable only for certain classes of applications and are criticized for the difficulty of extracting the desired level of performance: generating good circuits still requires tedious code restructuring and hardware design expertise. In this talk, I will present a new HLS methodology that produces dynamically scheduled, dataflow circuits out of C/C++ code; the resulting circuits achieve good performance out of the box and realize behaviors that are beyond the capabilities of standard HLS tools. I will outline mathematical models to optimize the performance and area of the resulting circuits, as well as techniques to achieve characteristics that standard HLS cannot support, such as out-of-order memory accesses and speculative execution. These contributions redefine the HLS paradigm by introducing characteristics of modern superscalar processors to hardware designs; such behaviors are key for specialized computing to be successful in new contexts and broader application domains.
Short bio: Lana Josipović is an Assistant Professor in the Department of Information Technology and Electrical Engineering at ETH Zurich. Prior to joining ETH Zurich in January 2022, she received a Ph.D. degree in Computer Science from EPFL, Switzerland. Her research interests include reconfigurable computing and electronic design automation, with an emphasis on high-level synthesis techniques to generate hardware designs from high-level programming languages. She developed Dynamatic, an open-source high-level synthesis tool that produces dynamically scheduled circuits from C/C++ code. She is a recipient of the EDAA Outstanding Dissertation Award, Google Ph.D. Fellowship in Systems and Networking, Google Women Techmakers Scholarship, and Best Paper Award at FPGA'20.

Name: Alessio Merlo
Job Title: Associate Professor, University of Genova
Title of the talk: Mining Anonymized Personal Data on Distributed Architectures
Abstract: When executing, applications keep gathering a lot of personal data through proper analytic libraries. Such data are sent to the application backend and analyzed by developers by leveraging data mining techniques with the aim to extract useful information for improving the quality of the provided functionality. Some data can also be sent to third parties for further mining activities. Users have normally no control over the acquisition of their personal data: nonetheless, data anonymization techniques can be used to reduce the amount of personal information that reach the backend. The net result is that the mining activity is negatively affected as the utility of data lowers. In this talk we discuss such data privacy vs. data utility dilemma, poiting out how both anonymization and data mining algorithms can scale over parallel and distributed architectures.
Short bio: Alessio Merlo (IEEE Senior Member) is an Associate Professor in Computer Engineering at the University of Genoa. His main research interests focus on Mobile Security

and Privacy. He is the director of the II level master in "Cybersecurity and Critical Infrastructure Protection" at the University of Genoa. He co-authored more than 120 papers on international journals and conferences.

Name: Jan Martinovic
Job title: Head of Research Lab, VSB-TU Ostrava, IT4Innovations
Title of the talk: From HPC-as-a-Service to LEXIS Platform
Abstract: HPC as a Service (HPCaaS) is a well-known term in the area of high-performance computing. It enables users to access an HPC infrastructure without a need to buy and manage their own infrastructure. Through this service, academia and industry can take advantage of the technology without an upfront investment in the hardware. This approach further lowers the entry barrier for users who are interested in utilizing massive parallel computers but often do not have the necessary level of expertise in the area of parallel computing. The lecture will introduce the HPCaaS concept. Then we will focus on the two concrete examples which leverage the HPCaaS concept. The first one is High-End Application Execution Middleware. This universally designed open-source software enables unified access to different HPC systems through a simple object-oriented REST API. The second one is the LEXIS Platform. This platform aims to overcome the shortcomings of complicated access to a high-performance computing system and management of large datasets by providing a clean and concise interface that abstracts both HPC and cloud resources using workflow and data management orchestration.
Short bio: Jan Martinovic, Ph.D. is currently the Head of the Advanced Data Analysis and Simulations Lab at IT4Innovations National Supercomputing Center. He has extensive experience of leading substantial R&D activities. His research activities are focused on HPC, Cloud and BigData convergence, HPC-as-a-Service, traffic management and data analysis. He coordinated of the ICT-11 project LEXIS (https://lexis-project.eu). In addition, he has previous experience with the management of different contracted research activities with international and national companies. He is participating in the ICT-51 EVEREST project, and EuroHPC projects LIGATE, IO-SEA and ACROSS. He was a leading researcher at IT4Innovations of the two H2020-FETHPC-2014 projects ANTAREX and ExCAPE. Jan is HiPEAC and IEEE member.

Name: Francesco Regazzoni
Job title: Tenured Assistant Professor at University of Amsterdam and Group Leader at Università della Svizzera italiana
Title of the talk: From local devices to large scale could computing: physical attacks on FPGAs
Abstract: The talk presents an introduction to physical attacks on FPGAs. After a quick presentation of physical attacks in general, this lecture presents how these attacks have been applied to reconfigurable hardware and the most common and effective ways to counteract them. The talk will cover the evolution of the threat, from the initial key recovery possible on devices physically accessed by the adversary, to the latest extraction of secret information from shared FPGAs on the cloud. The lecture will show how these attacks have been demonstrated to be practically feasible in real world settings, and will discuss possible directions for future research.
Short bio: Francesco Regazzoni is a tenured Assistant Professor at University of Amsterdam and group leader at Università della Svizzera italiana. He received his Master of Science degree from Politecnico di Milano and his PhD degree from Université della Svizzera italiana. He held research positions at the Université Catholique de Louvain and at Technical University of Delft, and has been visiting researcher at several institutions, including NEC Labs America, Ruhr University of Bochum, and EPFL Lausanne. His

research interests are mainly focused on secure IoT devices and embedded systems, covering in particular design automation for security, physical attacks and countermeasures, post-quantum cryptography, and efficient implementation of cryptographic primitives. He served on the technical program committed of top conferences of the area of security and design automation including CHES, DAC, DATE, ICCAD, and HOST, and has been co-chair of the technical program committee of FDTC 2017, COSADE 2020 and CCSW 2022.

Name: Christoph Hagleitner
Job title: Senior Research Scientist, IBM Research Europe
Title of the talk: CloudFPGA Research Platforms
Abstract: The SDK developed within the EVEREST project is built on and targets two distinct FPGA platforms, which are developed by IBM Research: 1) The CloudFPGA platform (https://github.com/cloudFPGA), which targets scale-out FPGA applications running in a cloud-environment and 2) The HPC FPGA platform targeting high-performance applications running on FPGAs within complex workflows, eg, the EVEREST use-cases. In this overview presentation, I will introduce the architecture and design of the two platform as well as the development environment needed to deploy applications.
Short bio: Christoph Hagleitner leads the cloudFPGA project at the IBM Research Europe Lab (ZRL) in Ruschlikon, Switzerland. He obtained a Ph.D. degree for a thesis on CMOS-integrated Microsensors from ETH, Zurich, Switzerland in 2002. In 2003 he joined IBM Research to work on the system architecture of a novel probe-storage device ("millipede"-project). In 2008, he started to build up a new research group in the area of accelerator technologies. The team initially focused on integrated accelerator cores and gradually expanded its research to heterogeneous computing systems and their applications.